

ABSTRACT OF THE DISCLOSURE

A ferroelectric memory device of the present invention includes a memory cell array in which memory cells are arranged
5 in a matrix having first signal electrodes, second signal
electrodes arranged in a direction intersecting the first
signal electrodes, and a ferroelectric layer disposed at least
in intersection regions between the first signal electrodes and
the second signal electrodes, and a peripheral circuit section
10 for selectively writing information into or reading information
from the memory cell. The memory cell array and the peripheral
circuit section are formed in different layers. The peripheral
circuit section is formed in a region outside the memory cell
array.